In the Claims:

1-59. (Canceled)

60. (Currently Amended) A method of forming a resistor, the method comprising:

providing a silicon-on-insulator substrate that includes a silicon layer overlying an insulator layer;

forming a resistor body of a first conductivity type in a portion of the silicon layer;

forming a dielectric layer overlying the body region, the dielectric layer comprising a material with a relative permittivity greater than about 8;

forming a top electrode on the dielectric layer, the top electrode comprising a conductive material; and

forming a pair of doped regions of the first conductivity type oppositely adjacent the body region.

61. (Original) The method of claim 60 wherein forming the resistor body comprises:

forming an active region;

forming isolation regions surrounding the active region; and

doping the active region.

62. (Original) The method of claim 61 wherein doping the active region employs an ion implantation with a dose in the range of about 10^{13} to about 10^{16} cm^{-2}.

63. (Original) The method of claim 60 wherein forming the dielectric layer comprises a chemical vapor deposition step.

64. (Withdrawn) The method of claim 60 wherein forming the dielectric layer comprises a sputtering deposition step.

65. (Original) The method of claim 60 wherein forming the dielectric layer comprises:
forming an interfacial oxide layer; and
forming a high permittivity dielectric layer.

66. (Original) The method of claim 60 wherein forming the pair of doped regions comprises:
doping a portion of the silicon layer not covered by the top electrode;
forming spacers on sidewalls of the top electrode; and
doping a portion of the silicon layer not covered by the top electrode and the spacers.

67. (Original) The method of claim 66 wherein the spacers comprise silicon nitride.

68. (Original) The method of claim 66 further comprising:
depositing an etch-stop layer over the top electrode and the spacers;
forming an inter-layer dielectric over the etch-stop layer;
forming contact holes in the inter-layer dielectric layer; and
filling the contact holes with a conductive material to form contact plugs.

69. (Original) The method of claim 68 wherein the etch-stop layer comprises silicon nitride.

70. (Original) The method of claim 68 wherein the inter-layer dielectric comprises silicon oxide.

71. (Original) The method of claim 68 wherein a first contact plug electrically contacts one of the pair of doped regions and a second contact plug electrically contacts the top electrode, said first and second contact plugs being electrically connected.

72. (Original) The method of claim 60 wherein the insulator layer comprises silicon oxide.

73. (Original) The method of claim 60 wherein the insulator layer has a thickness of less than about 1200 angstroms.

74. (Original) The method of claim 60 wherein the silicon layer has a thickness in the range of about 20 angstroms to about 1000 angstroms.

75. (Currently Amended) The method of claim 60 wherein the top electrode comprises a doped semiconductor.

76. (Withdrawn) The method of claim 60 wherein the top electrode comprises a metal selected from the group consisting of molybdenum, tungsten, titanium, tantalum, platinum, and hafnium.

77. (Withdrawn) The method of claim 60 wherein the top electrode comprises a metallic nitride selected from the group consisting of molybdenum nitride, tungsten nitride, titanium nitride, tantalum nitride, or combinations thereof.

78. (Withdrawn) The method of claim 60 wherein the top electrode comprises a metallic silicide selected from the group consisting of nickel silicide, cobalt silicide, tungsten silicide, titanium silicide, tantalum silicide, platinum silicide, and erbium silicide, and combinations thereof.

79. (Withdrawn) The method of claim 60 wherein the top electrode comprises a metallic oxide selected from the group comprising of ruthenium oxide, and indium tin oxide, and combinations thereof.

80. (Original) The method of claim 60 wherein the dielectric layer comprises a material selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, and zirconium silicate, and combinations thereof.

81. (Original) The method of claim 60 wherein the dielectric layer has a relative permittivity of larger than about 10.

82. (Original) The method of claim 60 wherein the dielectric layer has a relative permittivity of larger than about 20.

83. (Original) The method of claim 60 wherein the dielectric has a physical thickness greater than about 5 angstroms.

84. (Original) The method of claim 83 wherein the dielectric has a physical thickness greater than about 20 angstroms.

85. (Original) The method of claim 84 wherein the dielectric has a physical thickness greater than about 40 angstroms.

86. (Original) The method of claim 60 wherein the electrode has a width greater than about 0.1 microns.

87. (Original) The method of claim 60 wherein the electrode has a width greater than about 1 micron.

88. (Original) The method of claim 60 the electrode has a length greater than about 0.1 microns.

89. (Original) The method of claim 61 wherein the electrode has a length greater than about 1 micron.

90-115. (Canceled)